

REMARKS

The Office Action mailed October 8, 2002, has been received and reviewed. Claims 1 through 26 and 72 through 106 are currently pending in the application. Claims 1 through 26 and 72 through 106 stand rejected. Claims 1 through 26 and 72 through 102 have been objected to on the basis of certain writing informalities. Reconsideration is respectfully requested.

Information Disclosure Statement

Applicant notes the filing of a Supplemental Information Disclosure Statement on October 16, 2002. The Supplemental Information Disclosure Statement is again filed herein with the fee pursuant to 37 C.F.R. § 1.117(p) and Applicant respectfully requests that the information cited on the PTO/SB/08A be made of record.

Specification Objections

The Specification was objected to for using the term “metal layer” to mean “metal containing layer.” Applicant has made appropriate corrections in a substitute specification filed herewith. No new matter has been added.

Claim Objections Based Upon Writing Informalities

Claims 1 through 26 and 72 through 102 are objected to because of writing informalities. Applicant has amended the claims as suggested by the Examiner. Specifically, the claims have been amended to recite “metal containing spacers” where appropriate. Reconsideration and withdrawal of the objection is requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent 6,030,896 to Brown

Claims 1 through 11, 14 through 26, 72 through 89, and 92 through 106 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brown (U.S. Patent 6,030,896). Applicant respectfully traverses this rejection, as hereinafter set forth.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. § 103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. See M.P.E.P. 706.02(j).

Brown discloses a via formed in a semiconductor device. A first layer of dielectric material 10 is deposited on a semiconductor substrate. A first diffusion barrier layer 12 is formed on the dielectric material 10 and a layer of copper 14 is formed thereover. An etch stop/second barrier layer 16 is formed over the layer of copper 14 and a second copper layer 18 is formed thereover. A third barrier layer 20 is formed on the second copper layer 18 and the structure is patterned. A thin layer of conductive material 22 is formed over the third barrier layer 20 and etched to expose the third barrier layer 20. (Brown, FIG. 3.) A second dielectric layer 24 is deposited and planarized to expose third barrier layer 20. (Brown FIG. 4.)

By way of contrast with Brown, independent claim 1 of the presently claimed invention recites a "method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a single conducting layer over the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers being

substantially the same height as said multilayer structure.” Applicant respectfully submits that Brown fails to teach or suggest every element of claim 1 of the presently claimed invention.

Specifically, Brown fails to teach or suggest “a second dielectric layer in contact with the single conducting layer.” Instead, Brown teaches the second dielectric layer 24 in contact with sidewall spacers 22 that are formed of barrier metal materials. (Brown, col. 4, lines 65-67.) The second dielectric layer 24 does not contact either copper layer 14, 18. Accordingly, as Brown fails to teach or suggest every element of claim 1 of the presently claimed invention, applicant submits that Brown does not render the presently claimed invention obvious.

Claims 2 through 26 are each allowable as depending, either directly or indirectly, from allowable independent claim 1.

Claim 4 is further allowable as Brown fails to teach or suggest forming a second metal containing barrier layer between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

Claim 8 is further allowable as Brown fails to teach or suggest forming the single conducting layer comprises forming the single conducting layer of an aluminum-copper alloy.

Claim 11 is further allowable as Brown fails to teach or suggest forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

Claim 12 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a low dielectric constant material.

Claim 13 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a fluorine-doped silicon oxide.

Claim 15 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer by vapor deposition.

Claim 16 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

Claim 17 is further allowable as Brown fails to teach or suggest forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

Claim 18 is further allowable as Brown fails to teach or suggest forming the single conducting layer by CVD, PVD or PECVD.

Claim 21 is further allowable as Brown fails to teach or suggest removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the single conducting layer, and the at least one metal containing barrier layer. Instead, Brown discloses masking and patterning the third barrier layer 20, second copper layer 18, etch stop/ second barrier layer 16, first copper layer 14 and first barrier layer 12 and subsequently planarizing the second dielectric layer 24. (Brown, col. 4, lines 50-62; col. 5, lines 5-17.)

Claim 22 is further allowable as Brown fails to teach or suggest forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers. Instead, Brown discloses forming the conductive barrier material 22 before the second dielectric layer 24. (Brown, paragraph bridging col. 4 and 5; col. 5, lines 5-17.)

Claims 25 and 26 are further allowable as Brown fails to teach or suggest removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto to expose said single conducting layer. Instead, Brown discloses planarizing the second dielectric layer 24 and conductive barrier material 22 to expose a barrier metal layer 20.

By way of contrast with Brown, claim 72 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a single conducting layer over the at least one metal containing barrier layer; removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer."

Applicant respectfully submits that Brown fails to teach or suggest every element of the presently claimed invention. Specifically, Brown fails to teach or suggest "said metal containing spacer extending to substantially the same height as said single conducting layer." Instead, Brown discloses conductive barrier spacers 22 that extend above the conducting layer to substantially the same height as the diffusion barrier layer 20. (Brown, FIGs. 3 and 4.) As Brown fails to teach or suggest every element of the presently claimed invention, applicant submits that independent claim 72 of the presently claimed invention is not rendered obvious by Brown. Thus, claim 72 is allowable.

Claims 73 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

Claims 73 and 74 are further allowable as Brown fails to teach or suggest forming a second dielectric layer in direct contact with said single conducting layer. Instead, Brown discloses a dielectric layer 24 in contact with conductive barrier spacers 22. (Brown, FIG. 4.)

Claims 75 and 76 are further allowable as Brown fails to teach or suggest forming a metal containing spacer layer on said second dielectric layer and removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

Claim 81 is further allowable as Brown fails to teach or suggest forming a second metal containing barrier layer between a first metal containing barrier layer of the at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

Claim 84 is further allowable as Brown fails to teach or suggest creating the single conducting layer of an aluminum-copper alloy.

Claim 89 is further allowable as Brown fails to teach or suggest forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer. Instead Brown discloses a dielectric layer 24 in contact with conductive barrier spacers 22. (Brown, FIG. 4.)

Claim 90 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a low dielectric constant material.

Claim 91 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a fluorine-doped silicon oxide.

Claim 93 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer by vapor deposition.

Claim 94 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

Claim 95 is further allowable as Brown fails to teach or suggest forming the conducting layer by vapor deposition.

Claim 96 is further allowable as Brown fails to teach or suggest forming the single conducting layer by CVD, PVD or PECVD.

Claim 99 is further allowable as Brown fails to teach or suggest that removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure is effected by patterning and etching the single conducting layer and the at least one metal containing barrier layer. Instead, Brown discloses masking and patterning the third barrier layer 20, second copper layer 18, etch stop/ second barrier layer 16, first copper layer 14 and first barrier layer 12 and subsequently planarizing the second dielectric layer 24. (Brown, col. 4, lines 50-62; col. 5, lines 5-17.)

Claim 100 is further allowable as Brown fails to teach or suggest that flanking comprises forming the metal containing spacer by forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

Independent claim 103 is allowable for substantially the same reasons as allowable claim 1. By way of contrast with Brown, claim 103 of the presently claimed invention recites a "method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a conducting layer over the at least one metal containing barrier layer; forming a second dielectric layer in contact with the conducting layer; removing aligned portions of the second dielectric layer, conducting layer, and at least one metal containing barrier layer to form a multilayer structure; forming metal containing spacers on sidewalls of the multilayer structure; and removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto."

Applicant respectfully submits that Brown fails to teach or suggest every element of the presently claimed invention. Specifically, Brown fails to teach or suggest forming a second dielectric layer in contact with the conducting layer. Instead, Brown teaches the second dielectric layer 24 in contact with sidewall spacers 22 that are formed of barrier metal materials. (Brown, col. 4, lines 65-67.) The second dielectric layer 24 does not contact either copper layer 14, 18. Accordingly, as Brown fails to teach or suggest every element of claim 103 of the presently claimed invention, applicant submits that Brown does not render the presently claimed invention obvious.

Claim 104 is allowable as depending from allowable claim 103 of the presently claimed invention.

Independent claim 105 is allowable for substantially the same reasons as allowable claim 72. By way of contrast with Brown, claim 105 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating a

conducting layer over the at least one metal containing barrier layer; removing aligned portions of the conducting layer and at least one metal containing barrier layer to form a multilayer structure; flanking at least one surface of the multilayer structure with a metal containing spacer such that said metal containing spacer is substantially the same height as said conducting layer; and removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.”

Applicant respectfully submits that Brown fails to teach or suggest “flanking at least one surface of the multilayer structure with a metal containing spacer such that said metal containing spacer is substantially the same height as said conducting layer.” Instead, Brown discloses conductive barrier spacers 22 that extend above the conducting layer to substantially the same height as the diffusion barrier layer 20. (Brown, FIGs. 3 and 4.) As Brown fails to teach or suggest every element of the presently claimed invention, applicant submits that independent claim 105 of the presently claimed invention is not rendered obvious by Brown. Thus, claim 105 is allowable.

Claim 106 is allowable as depending from allowable claim 105.

Obviousness Rejection Based on U.S. Patent 6,277,745 to Liu et al.

Claims 1, 11 through 13, 72 through 75, and 88 through 91 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent 6,277,745). Applicant respectfully traverses this rejection, as hereinafter set forth.

Liu discloses a passivation method of post copper dry etching. Liu discloses a sandwich structure consisting of a bottom barrier layer 4, a copper layer 6 and a top barrier metal layer 8. After formation of this sandwich structure and patterning, the exposed sidewalls are passivated by means of a barrier metal spacer process. Liu teaches that the fully encapsulated copper lines are highly resistant to oxidation which is an otherwise inherent problem with bare copper lines. (Liu, Abstract.)

By way of contrast with Liu, claim 1 of the presently claimed invention recites a method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the

first dielectric layer; forming a single conducting layer over the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers being substantially the same height as said multilayer structure.

Applicant respectfully submits that Liu fails to teach or suggest every element of the presently claimed invention. Specifically, Liu fails to teach or suggest forming a second dielectric layer in contact with the single conducting layer or forming a substantially planar first dielectric layer on a substrate. Instead, Liu discloses a lower barrier metal layer 4, copper conducting layer 6, an overlying barrier metal layer 8 and a hard mask layer 16. The hard mask layer 16 of Liu contacts the barrier metal layer 8. Applicant respectfully disagrees with the examiner's statement that the barrier metal layer 8 of Liu comprises a conducting layer. (See, Paper No. 12, page 6 and Liu, col. 3, lines 30-41.) Liu teaches the metal barrier layer 8 comprises materials such as TaN, TiN or Ta which functions are as barrier metal layer, not a conducting layer. (Liu, col. 3, lines 39-41.)

Accordingly, Liu fails to teach or suggest every element of independent claim 1. As such, claim 1 is allowable.

Claims 2 through 26 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 11 is further allowable as Liu fails to teach or suggest forming the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Independent claim 72 of the presently claimed invention is allowable for substantially the same reasons as independent claim 1. Claim 72 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating

a single conducting layer over the at least one metal containing barrier layer; removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer."

Applicant respectfully submits that Liu fails to teach or suggest "providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer" or "flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer." Instead, Liu discloses spacers extending to either the same height as the hard mask layer 16 or the second barrier metal layer 8. (Liu, Figs. 1D and 2D.) As Liu fails to teach or suggest every element of the presently claimed invention, claim 72 is not rendered obvious in view of Liu. Thus, claim 72 is allowable.

Claims 73 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

Claim 73 is further allowable as Liu fails to teach or suggest forming a second dielectric layer in contact with said conducting layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Claim 89 is further allowable as Liu fails to teach or suggest forming the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Obviousness Rejection Based on U.S. Patent 6,074,943 to Brennan et al.

Claims 1 through 12, 14 through 24, 72 through 75, 78 through 90, and 92 through 102 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brenna[n] et al. (U.S. Patent 6,074,943). Applicant respectfully traverses this rejection, as hereinafter set forth.

Brennan discloses a method of forming via structures using sidewalls as guides. Thus, as shown in FIG. 2H, Brennan discloses an Al-Cu layer 210 overlying an oxide layer 200 and an optional TiN barrier layer 205. A layer of anti-reflective coating (TiN) 215 is deposited on the Al-Cu layer 210. While Brennan teaches that the TiN barrier layer 205 is optional, it does not state that the anti-reflective coating 215 is optional. (Brennan, col. 2, lines 37-42.) A layer of sidewall material 240 is deposited (FIG. 2E) and etched to an etch stop layer 220. The etch stop layer 220 is removed and a dielectric material 250 is deposited over the structure in contact with and sidewalls 240. (FIG. 2G.) Brennan teaches that after the dielectric material 250 deposition is complete, “the sidewall material 240 will jut up into the ILD 250, forming sidewall extensions 260.” (Brennan, col. 2, lines 64-66.) Subsequently, vias 270 are etched in the ILD layer 250 to contact the underlying interconnect. (FIG. 2H.)

Applicant respectfully submits that Brennan fails to teach or suggest every element of the presently claimed invention. By way of contrast with Brennan, claim 1 of the presently claimed invention recites a “method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a single conducting layer over the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers being substantially the same height as said multilayer structure.”

Applicant respectfully submits that Brennan fails to teach or suggest “forming a second dielectric layer in contact with the single conducting layer.” Instead, Brennan teaches a dielectric layer 250 in contact with sidewalls 260 and an upper barrier metal layer 215. (Brennan, cols. 4-5, lines 63-14; FIGs. 2G, 2H.) Further, Brennan fails to teach or suggest “forming at least one metal containing barrier layer over the first dielectric layer” or “forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers being substantially the same

height as said multilayer structure.” (Brennan, FIG. 2H.) Applicant submits that the intermediate product shown in FIG. 2F of Brennan is not the multilayer structure of claim 1 of the presently claimed invention. Specifically, claim 1 of the presently claimed invention recites “removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal spacers being substantially the same height as said multilayer structure.” By way of contrast, the intermediate product shown in FIG. 2F of Brennan is not formed by removing a second dielectric layer.

As Brennan fails to teach or suggest every element of claim 1 of the presently claimed invention, applicant respectfully submits that claim 1 is not rendered obvious by Brennan. Accordingly, claim 1 is allowable.

Claims 2 through 26 are each allowable as depending, either directly or indirectly from allowable claim 1.

Claim 2 is further allowable as Brennan fails to teach or suggest forming a silicon oxide or BPSG layer.

Claim 11 is further allowable as Brennan fails to teach or suggest forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

Claim 15 is further allowable as Brennan fails to teach or suggest forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

Claim 16 is further allowable as Brennan fails to teach or suggest forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

Claim 17 is further allowable as Brennan fails to teach or suggest forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

Claim 18 is further allowable as Brennan fails to teach or suggest forming the single conducting layer by CVD, PVD or PECVD.

Claim 21 is further allowable as Brennan fails to teach or suggest removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the single conducting layer, and the at least one metal containing barrier layer.

Claim 22 is further allowable as Brennan fails to teach or suggest forming the metal containing spacers comprises forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

Independent claim 72 is allowable for substantially the same reasons as claim 1. By way of contrast with Brennan, claim 72 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating a single conducting layer over the at least one metal containing barrier layer; removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer."

Applicants respectfully submit that Brennan fails to teach or suggest "providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer" or "flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer." Instead, Brennan discloses creating spacers that extend beyond a conducting layer 210 and beyond a barrier layer 215 to substantially the same height as a hard mask layer 220. (Brennan FIG. 2f.) Alternatively, Brennan discloses spacers that extend beyond the multilayer structure to act as guides. Brennan teaches that after the dielectric material 250 deposition is complete, "the sidewall material 240 will jut up into the ILD 250, forming sidewall extensions 260." (Brennan, col. 2, lines 64-66.) Subsequently, vias 270

are etched in the ILD layer 250 to contact the underlying interconnect. (FIG. 2H.) As Brennan fails to teach or suggest every element of the presently claimed invention, applicant submits that claim 72 is not rendered obvious by Brennan. Thus, claim 72 is allowable.

Claims 73 through 102 are each allowable as depending either directly or indirectly from claim 72.

Claim 73 is further allowable as Brennan fails to teach or suggest forming a second dielectric layer in contact with said single conducting layer.

Claim 74 is further allowable as Brennan fails to teach or suggest that removing further comprises removing aligned portions of said second dielectric layer to form said multilayered structure.

Claim 76 is further allowable as Brennan fails to teach or suggest removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

Claim 78 is further allowable as Brennan fails to teach or suggest that providing a substrate having a first dielectric layer comprises forming said first dielectric layer of a silicon oxide or BPSG layer.

Claim 89 is further allowable as Brennan fails to teach or suggest forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer.

CONCLUSION

Claims 1 through 26 and 72 through 106 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully Submitted,



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KWP/hlg:lb/csw

Enclosure: Appendix A: Clean Version of Substitute Specification
Appendix B: Version of Substitute Specification with Markings to Show Changes
Made
Appendix C: Version of Claims Amended Herein with Markings to Show Changes
Made

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APPENDIX C

**(VERSION OF CLAIMS AMENDED HEREIN
WITH MARKINGS TO SHOW CHANGES MADE)**

(Serial No. 09/829,161)

APPENDIX C

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended three times) A method for making a metallization structure for a semiconductor device, comprising:
forming a substantially planar first dielectric layer on a substrate;
forming at least one metal containing barrier layer over the first dielectric layer;
forming a single conducting layer over the at least one metal containing barrier layer;
forming a second dielectric layer [over] in contact with the single conducting layer;
removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and
forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers being substantially the same height as said multilayer structure.
3. (Amended three times) The method of claim 2, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.
4. (Amended four times) The method of claim 3, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.
5. (Amended three times) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

6. (Amended twice) The method of claim 1, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

9. (Amended twice) The method of claim 1, wherein said forming the metal containing spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

10. (Amended twice) The method of claim 9, wherein said forming the metal containing spacers comprises forming the metal containing spacers of titanium or titanium nitride.

11. (Amended three times) The method of claim 1, wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

14. (Amended twice) The method of claim 1, further comprising forming the at least one metal containing barrier layer and the metal containing spacers of a same metal.

15. (Amended three times) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

16. (Amended four times) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

19. (Amended twice) The method of claim 1, wherein said forming the metal containing spacers comprises forming the metal containing spacers by vapor deposition and directional etching.

21. (Amended three times) The method of claim 1, wherein removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the single conducting layer, and the at least one metal containing barrier layer.

22. (Amended three times) The method of claim 1, wherein said forming the metal containing spacers comprises forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

23. (Amended three times) The method of claim 22, wherein said forming the metal containing spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer by a conformal deposition process.

24. (Amended twice) The method of claim 23, wherein portions of the metal containing spacer layer over the multilayer structure and first dielectric layer are removed by etching.

25. (Amended twice) The method of claim 1, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto to expose said single conducting layer.

26. (Amended twice) The method of claim 25, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers by etching.

72. (Amended twice) A method for constructing a metallization structure for a semiconductor device, comprising:
providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;
creating a single conducting layer over the at least one metal containing barrier layer;
removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and
flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer [being] extending to substantially the same height as said [multilayer structure] single conducting layer.

73. (Amended twice) The method of claim 72, further comprising forming a second dielectric layer [over] in contact with said single conducting layer.

75. (Amended) The method of claim 73, wherein said flanking at least one surface of the multilayer structure with a metal containing spacer comprises forming a metal containing spacer layer on said second dielectric layer.

76. (Amended) The method of claim 75, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

79. (Amended twice) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

80. (Amended twice) The method of claim 79, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

81. (Amended twice) The method of claim 72, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of the at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

82. (Amended twice) The method of claim 72, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

85. (Amended) The method of claim 72, wherein said flanking comprises forming the metal containing spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

86. (Amended) The method of claim 85, wherein said forming the metal containing spacer comprises forming the metal containing spacers of titanium or titanium nitride.

87. (Amended twice) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on sidewalls of said multilayer structure.

88. (Amended) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on a top surface of said multilayer structure.

89. (Amended twice) The method of claim 72, further comprising forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer.

92. (Amended twice) The method of claim 72, further comprising forming the at least one metal containing barrier layer and the metal containing spacer of a same metal.

93. (Amended twice) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

94. (Amended twice) The method of claim 93, wherein said forming the at least one metal containing barrier layer by vapor deposition comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

97. (Amended) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by vapor deposition and directional etching.

99. (Amended twice) The method of claim 72, wherein removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure is effected by patterning and etching the single conducting layer and the at least one metal containing barrier layer.

100. (Amended) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

101. (Amended twice) The method of claim 100, wherein said forming the metal containing spacer layer over the multilayer structure and first dielectric layer comprises forming the metal containing layer by a conformal deposition process.

102. (Amended) The method of claim 101, wherein said removing portions of the metal containing spacer layer is effected by etching.

103. (Amended) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;
forming at least one metal containing barrier layer over the first dielectric layer;
forming a conducting layer over the at least one metal containing barrier layer;
forming a second dielectric layer [over] in contact with the conducting layer;
removing aligned portions of the second dielectric layer, conducting layer, and at least one metal containing barrier layer to form a multilayer structure;
forming metal containing spacers on sidewalls of the multilayer structure; and
removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto.

105. (Amended) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a conducting layer over the at least one metal containing barrier layer;

removing aligned portions of the conducting layer and at least one metal containing barrier layer to form a multilayer structure;

flanking at least one surface of the multilayer structure with a metal containing spacer such that

said metal containing spacer is substantially the same height as said conducting layer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.



APPENDIX A

(CLEAN VERSION OF SUBSTITUTE SPECIFICATION EXCLUDING CLAIMS)

(Serial No. 09/829,161)

PATENT
Attorney Docket 3442.1US (96-428.1)

NOTICE OF EXPRESS MAILING

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APPLICATION FOR LETTERS PATENT

for

**METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE
INTERCONNECTS, METHODS FOR MAKING SAME, AND
SEMICONDUCTOR DEVICES INCLUDING SAME**

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TITLE OF THE INVENTION

METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS,
METHODS FOR MAKING SAME, AND
SEMICONDUCTOR DEVICES INCLUDING SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of application Serial No. 09/388,031, filed September 1, 1999, pending.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: This invention relates generally to the field of semiconductor device design and fabrication. Specifically, the invention relates to methods for manufacturing metallization structures in integrated circuit devices and the resulting structures.

[0003] State of the Art: Integrated circuits (ICs) contain numerous individual devices, such as transistors and capacitors, that are interconnected by an intricate network of horizontal and vertical conductive lines commonly termed "interconnects." Exemplary interconnect structures are disclosed in U.S. Patent Nos. 5,545,590, 5,529,954, 5,300,813, 4,988,423, and 5,356,659, each of which patents is hereby incorporated herein by reference.

[0004] Aluminum interconnect structures are decreasing in size and pitch (spacing), as the industry trend continues toward, and includes, submicron features and pitches. The resultant reduction in structure sizes leads to numerous reliability concerns, including electromigration and stress voiding of the interconnect structures.

[0005] Stress notches (also known as stress voids) on the surface of conductive interconnect structures are of concern because the voids or notches degrade reliability and device performance. Stress notches, when formed in a conductive line, may render the line substantially discontinuous and unable to effectively transmit a signal. Stress notches at a grain boundary are extremely detrimental, as they may propagate along the boundary and sever the conductive line completely.

[0006] Stress notches are also undesirable because they can alter the resistivity of a conductive line and change the speed at which signals are transmitted. Resistivity changes from stress notching are especially important as line dimensions shrink, because notching in a submicron conductive line alters resistivity more than notching in a larger line with its consequently greater cross-sectional area. Thus, the ever more stringent pitch sizing and higher aspect ratios (height to width of the structure or feature) sought by practitioners in the art have imitated considerable stress voiding concerns.

[0007] It is believed that stress notching results from both structural and thermal stresses between conductive lines and adjacent insulating and passivation layers. Kordic et al., *Size and Volume Distributions of Thermally Induced Stress Voids in AlCu Metallization*, Appl. Phys. Lett., Vol. 68, No. 8, 19 February 1996, pp. 1060-1062, incorporated herein by reference, describes how stress voids begin at the edge of a conductive line where the density of the grain boundaries is largest. As illustrated in Figure 12 herein, stress notches form at the exterior surfaces and surface intersections of the conductive lines in order to relieve areas of high stress concentration. The notches may then propagate into, and across, the interior of the conductive line until the line becomes disrupted, cracked, and/or discontinuous.

[0008] Aluminum (Al) and Al alloy (such as Al/Cu) lines are especially susceptible to stress notching because of both the thermal expansion mismatch between Al and adjacent layers and the relatively low melting point of Al. As the temperature changes, stresses are induced in Al or Al alloy lines because aluminum's coefficient of thermal expansion (CTE) differs from the CTE of the materials comprising the adjacent layers. To relieve these stresses, Al atoms migrate and form stress notches. Further, because Al has a low melting point, Al atoms migrate easily at low temperatures and aggravate a tendency toward stress notch formation.

[0009] Several methods have been proposed to reduce stress notching. One proposed method uses a material less susceptible to stress notching, such as copper (Cu) or tungsten (W), in the conductive line. Using Cu in conductive lines, however, has in the past resulted in several problems. First, copper is difficult to etch. Second, adhesion between copper and adjacent insulating layers is poor and thus poses reliability concerns. Third, adding Cu to Al lines may reduce stress notching, but beyond a certain Cu concentration, device performance may begin to

degrade. Fourth, as conductive line geometries shrink, adding Cu to Al lines seems less effective in reducing stress notching. Finally, even using Cu interconnects in the manner employed in the prior art can still lead to notching effects, especially at $0.1 \mu\text{m}$ geometries and below since, at such dimensions, line widths have become so small that any imperfection can cause opens. Using W in Al conducting lines is also undesirable – W has a high resistivity and, therefore, reduces signal speed.

[0010] Another proposed method to reduce stress notching modifies how the layers adjacent conductive lines (e.g., insulating and passivation layers) are formed. This method has focused, without notable success, on the rate, temperature, and/or pressure at which the adjacent layers are deposited, as well as the chemical composition of such layers.

[0011] Yet another proposed method to reduce stress notching comprises forming a cap on the conductive lines. Such caps can be formed from TiN, W, or Ti-W compounds. These materials have higher melting points than Al and, therefore, have a higher resistance to stress notching. A disadvantage in using such caps, however, is that additional process steps, such as masking steps, are required.

[0012] U.S. Patent No. 5,317,185, incorporated herein by reference, describes still another proposed method for reducing stress notching. This patent discloses an IC device having a plurality of conductive lines where the outermost conductive line is a stress-reducing line. This stress-reducing line is a nonactive structure which reduces stress concentrations in the inner conductive lines.

BRIEF SUMMARY OF THE INVENTION

[0013] The present invention relates to a metallization structure for semiconductor device interconnects comprising a substrate having a substantially planar upper surface, a metal containing layer disposed on a portion of the substrate upper surface, a conducting layer overlying the metal containing layer, and metal containing spacers flanking the sidewalls of the conducting layer and the underlying metal containing layer. The metal containing layer and metal containing spacers do not encapsulate the conducting layer. The substrate upper surface is preferably a dielectric layer. The conducting layer preferably comprises aluminum or an

aluminum-copper alloy, but may also comprise copper. When the conducting layer comprises Al, the metal containing layer and metal containing spacer preferably comprise titanium, such as Ti or TiN. An optional dielectric layer, preferably silicon oxide, may be disposed on the conducting layer. When the optional dielectric layer is present, the metal containing spacer extends along the sidewall of the dielectric layer.

[0014] The present invention also relates to a metallization structure comprising a substrate having a metal containing layer disposed thereon, a dielectric layer having an aperture therethrough disposed on the substrate so the bottom of the aperture exposes the upper surface of the metal containing layer, at least one metal containing spacer on the sidewall of the aperture, and a conducting layer filling the remaining portion of the aperture. The metal containing layer and metal containing spacer preferably comprise titanium, such as Ti or TiN. At least one upper metal containing layer may be disposed on the conducting layer.

[0015] The present invention further relates to a method for making a metallization structure by forming a substantially planar first dielectric layer on a substrate, forming a metal containing layer over the first dielectric layer, forming a conducting layer over the metal containing layer, forming a second dielectric layer over the conducting layer, removing a portion of the second dielectric layer, conducting layer, and metal containing layer to form a multi-layer structure, and forming metal containing spacers on the sidewalls of the multi-layer structure. The process optionally removes both the second dielectric layer portion of the multi-layer structure and the laterally adjacent portions of the metal containing spacers.

[0016] The present invention additionally relates to a method for making a metallization structure by forming a substrate comprising a metal containing layer disposed thereon, forming a dielectric layer comprising an aperture on the substrate so the bottom of the aperture exposes the upper surface of the metal containing layer, forming a metal containing spacer on the sidewall (in the case of a via) or sidewalls (in the case of a trench) of the aperture, and forming a conducting layer in the remaining portion of the aperture. At least one upper metal containing layer may optionally be formed on the conducting layer.

[0017] The present invention also relates to a method for making a metallization structure by forming a substrate comprising a metal containing layer on the surface thereof,

forming on the substrate a dielectric layer comprising an aperture so the bottom of the aperture exposes the surface of the metal containing layer, forming a conducting layer in the aperture, forming an upper metal containing layer overlying the dielectric layer and the aperture, removing the portions of the upper metal containing layer overlying the dielectric layer, removing the dielectric layer, removing the portions of the metal containing layer not underlying the aperture to form a multi-layer metal containing structure, and forming a metal spacer on the sidewall or sidewalls of the multi-layer metal containing structure.

[0018] The present invention provides several advantages when compared to the prior art. One advantage is that thermally-induced stress voids are reduced because the metal containing layer and metal containing spacer comprise materials exhibiting good thermal-voiding avoidance characteristics. Another advantage is that the size of conductive lines can be shrunk further in comparison to dimensions achievable by conventional processes, since only one additional deposition and etch step, without an additional masking step, is needed to form the metallization structure. Shrinking of conductive lines is necessary as device geometries decrease to less than $0.1 \mu\text{m}$. At these small geometries, even small notches can significantly decrease conductivity.

[0019] The invention also specifically includes semiconductor devices including the inventive metallization structures.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0020] The present invention, in part, is illustrated by the accompanying drawings in which:

[0021] Figures 1, 2, 3a, and 3b illustrate cross-sectional views of one process of forming a metallization structure, and the structure formed thereby, according to the invention;

[0022] Figures 4, 5, 6, 7a, and 7b illustrate cross-sectional views of another process of forming a metallization structure, and the structure formed thereby, according to the invention;

[0023] Figures 8 and 9 illustrate cross-sectional views of yet another process of forming a metallization structure, and the structure formed thereby, according to the invention;

[0024] Figures 10 and 11 illustrate cross-sectional views of still another process of forming a metallization structure, and the structure formed thereby, according to the invention; and

[0025] Figure 12 illustrates a partial cross-sectional, perspective view of a conventional, prior art metallization structure exhibiting stress voids or notches.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Generally, the present invention relates to a metallization structure for interconnects and semiconductor devices including same. Specifically, the present invention reduces stress voiding, especially thermally induced stress voiding, in conducting lines. The metallization structures described below exemplify the present invention without reference to a specific device because the inventive process and structure can be modified by one of ordinary skill in the art for any desired device.

[0027] The following description provides specific details, such as material thicknesses and types, in order to provide a thorough description of the present invention. The skilled artisan, however, would understand that the present invention may be practiced without employing these specific details. Indeed, the present invention can be practiced in conjunction with conventional fabrication techniques employed in the industry.

[0028] The process steps described below do not form a complete process flow for manufacturing IC devices. Further, the metallization structures described below do not form a complete IC device. Only the process steps and structures necessary to understand the present invention are described below.

[0029] One embodiment of a process and resulting metallization structure of the present invention is illustrated in Figures 1, 2, 3a, and 3b. This embodiment may be characterized as a predominantly “subtractive” process, in comparison to the second embodiment discussed hereinafter, in that portions of superimposed material layers are removed to define the interconnect structure features, such as lines. As shown in Figure 1, a portion of semiconductor device 2 includes substrate 4 with overlying first dielectric layer 6. Substrate 4 may be any surface suitable for integrated circuit device formation, such as a silicon or other semiconductor

wafer or other substrate, and may be doped and/or include an epitaxial layer. Substrate 4 may also be an intermediate layer in a semiconductor device, such as a metal containing contact layer or an interlevel dielectric layer. Preferably, substrate 4 is a silicon wafer or bulk silicon region, such as a silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) structure.

[0030] First dielectric layer 6 may comprise any dielectric material used in IC device fabrication. Examples of such dielectric materials include silicon oxide, silicon nitride, silicon oxynitride, silicon oxide containing dopants such as boron (B) or phosphorus (P), organic dielectrics, or a layered dielectric film of these materials. Preferably, first dielectric layer 6 is silicon oxide or borophosphosilicate glass (BPSG). First dielectric layer 6 may be formed by any process yielding the desired physical and chemical characteristics, such as thermal oxidation, thermal nitridation, or vapor deposition.

[0031] Overlying first dielectric layer 6 is metal containing layer 8. One or more individual metal containing layers may be used as metal containing layer 8. For example, if two superimposed metal containing layers are employed (represented by the dashed line in metal containing layer 8), an adhesion-promoting metal containing layer can be a first, lower portion of metal containing layer 8 on first dielectric layer 6 and a stress-reducing layer can be a second, upper portion of metal containing layer 8. Other metal containing layers might be included for other functions, such as a layer for reducing electromigration. Preferably, a single metal containing layer is used as metal containing layer 8, especially when the single layer can reduce electromigration, function as an adhesion-promoting layer, and function as a stress-reducing layer. If two metal containing layers are employed, the first, upper metal containing layer may, for example, comprise tantalum, titanium, tungsten, TaN, or TiN and the second, lower metal containing layer overlying first dielectric layer 6 may, for example, comprise TiN, TiW, WN, or TaN.

[0032] Metal containing layer 8 includes not only metals, but their alloys and compounds (e.g., nitrides and silicides). For example, a metal containing layer containing titanium might also contain nitrogen or silicon, such as titanium nitride or titanium silicide. Any metal, metal alloy, or metal compound can be employed in metal containing layer 8, provided it exhibits the characteristics described above, either alone or when combined with other metal

containing layers. Examples of metals that can be employed in metal containing layer 8 include cobalt (Co), Ti, W, Ta, molybdenum (Mo), and alloys and compounds thereof, such as TiW or TiN. Preferably, metal containing layer 8 comprises titanium. Titanium is a good adhesion layer and serves as a stress-reducing layer since Ti exhibits good thermal voiding resistance characteristics.

[0033] Metal containing layer 8 is deposited or otherwise formed by any process used in IC device fabrication. For example, metal containing layer 8 may be deposited by chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques, depending on the characteristics required of the layer. As used herein, the term "CVD techniques" encompasses, without limitation, plasma-enhanced CVD, or PECVD. Preferably, when metal containing layer 8 is Ti, this layer is formed by sputtering (a form of PVD) a film of Ti. If metal containing layer 8 is a metal nitride, it may be formed, for example, by depositing the metal in a nitrogen-containing atmosphere or by depositing the metal and annealing in a nitrogen-containing atmosphere. If metal containing layer 8 is a metal silicide, it may be formed, for example, by first depositing either the metal containing layer or a silicon layer, then depositing the other, and heating to react the two layers and form the silicide. If metal containing layer 8 is a metal alloy, it may be formed by any process suitable for depositing the metal alloy. For example, either sputtering or CVD techniques can be employed.

[0034] Conducting layer 10 is then formed over metal containing layer 8. Conducting layer 10 may comprise any conducting material used in IC device fabrication. Preferably, conducting layer 10 comprises a conducting metal, such as Al, optionally containing other elements such as Si, W, Ti, and/or Cu. More preferably, conducting layer 10 is an aluminum-copper alloy. Conducting layer 10 may also be formed of Cu. Conducting layer 10 may be formed by any method used in IC device fabrication such as CVD or PVD techniques. Preferably, conducting layer 10 is deposited by a PVD method such as sputtering, as known in the art. Second dielectric layer 12 is next deposited or otherwise formed on top of conducting layer 10. Second dielectric layer 12 comprises any dielectric material used in IC device fabrication, including those listed above. Preferably, second dielectric layer 12 comprises a material that serves as an etch stop, as explained below. More preferably, second dielectric

layer 12 comprises fluorine-doped silicon oxide or other low dielectric constant material. Second dielectric layer 12 may be formed by any suitable process giving the desired physical and chemical characteristics, such as CVD, PECVD (plasma enhanced chemical vapor deposition), spin-on methods, or otherwise, depending upon the dielectric material selected. For use of the preferred fluorine-doped silicon oxide, the preferred deposition method is PECVD.

[0035] As shown in Figure 2, portions of second dielectric layer 12, conducting layer 10, and metal containing layer 8 have been removed, forming multi-layer structure 13. The portions of layers 8, 10 and 12 are removed by any IC device fabrication process, such as a photolithographic patterning and dry etching process. The resulting multi-layer structure forms the basis for an interconnect structure according to the present invention. Of course, the patterning and etch process would normally be performed to define a large number of interconnect structures, such as conductive lines 100 (see Figures 3a and 3b) extending across substrate 4.

[0036] As also shown in Figure 2, second metal containing layer 14 (also termed a metal containing spacer layer) is then deposited on first dielectric layer 6 and over multi-layer structure 13. In similar fashion to the structure of metal containing layer 8, one or more individual metal containing layers, illustrated by the dashed line within second metal containing layer 14, may be used as second metal containing layer 14. Preferably, a single metal containing layer is used as second metal containing layer 14 for the same reasons as those set forth for metal containing layer 8.

[0037] Like metal containing layer 8, second metal containing layer 14 includes not only metals but their alloys and compounds (e.g., nitrides and silicides). Preferably, when conducting layer 10 comprises aluminum, second metal containing layer 14 comprises Ti. If conducting layer 10 comprises Cu, second metal containing layer 14 preferably comprises TiW. More preferably, second metal containing layer 14 comprises the same metal as metal containing layer 8. Second metal containing layer 14 may be deposited or otherwise formed by a process similar to the process used to form metal containing layer 8. Preferably, second metal containing layer 14 is formed by a conformal deposition process, such as CVD.

[0038] Next, as illustrated in Figure 3a, second metal containing layer 14 is spacer etched to remove portions of the second metal containing layer 14 on first dielectric layer 6 and on second dielectric layer 12, thereby leaving metal containing spacers 16 on the multi-layer structure 13. A spacer etch is a directional sputtering etch which removes second metal containing layer 14 so that metal containing spacers 16 remain on the sidewalls of multi-layer structure 13. The spacer etch uses the first and second dielectric layers as an etch stop.

[0039] If desired, second dielectric layer 12 can then be removed. Second dielectric layer 12 can be removed by any process which removes the second dielectric layer without removing first dielectric layer 6. If the first and second dielectric layers comprise different materials (e.g., when second dielectric layer 12 is silicon oxide and the first dielectric layer 6 is BPSG), any process which selectively etches the second dielectric layer 12 can be employed. The etch process would also remove the portions of metal containing spacers 16 laterally adjacent dielectric layer 12, thus resulting in the metallization structure illustrated in Figure 3b. When the first and second dielectric layers 6, 12 are similar or have similar etch rates (e.g., when both are silicon oxide or fluorine-doped), a facet etch process can be used. As shown in broken lines in Figure 3b, when the first and second dielectric layers 6 and 12 exhibit similar etch rates, the thickness of layer 6 will be reduced by substantially the thickness of removed layer 12.

[0040] The metallization structures illustrated in Figures 3a and 3b reduce thermally-induced stress voids in conductive lines 100. Metal containing layer 8 and metal containing spacers 16 serve as a protective coating at the respective lower and lateral surfaces of conductive lines 100 and at intersections thereof, thereby reducing the incidence of stress voids by preventing them from starting at these surfaces and intersections thereof on conductive line 100. Metal containing layer 8 and metal containing spacers 16 also increase reliability of conductive line 100 without reducing its resistance.

[0041] The metallization structures of Figures 3a and 3b can then be processed as desired to complete the IC device. For example, an interlevel dielectric layer could be deposited thereover, contact or via holes could be cut in the interlevel dielectric, a patterned metal containing layer could be formed to achieve a desired electrical interconnection pattern, and a protective dielectric overcoat deposited and patterned to expose desired bond pads.

[0042] Another embodiment of a process and resulting metallization structures of the present invention is represented in Figures 4 through 11. This embodiment may be characterized as more of an "additive" method or process than that described with respect to Figures 1 through 3b, in that metallization structures for interconnects are formed by deposition in apertures, such as vias or trenches. As such, it should be noted that cusping of material deposited to line the sidewall or sidewalls of an aperture may be of concern if the method of deposition is not sufficiently anisotropic or, in some instances, the aperture exhibits a very high aspect ratio. In Figure 4, metal containing layer 52 has been deposited or otherwise formed over substrate 50. Any of the substrates employable as substrate 4 above can be used as substrate 50. Preferably, substrate 50 is a silicon wafer or bulk silicon region, such as an SOI or SOS structure. Such substrate 50 can have active and passive devices and other electrical circuitry fabricated on it, these circuit structures being interconnected by the metallization structures of the present invention. Therefore, a direct electrical path may exist between the devices and circuitry of the substrate 50 (or 4), the devices and circuitry being omitted herein for simplicity.

[0043] Metal containing layer 52 may comprise a discrete conductive member, such as a wire, a stud, or a contact. Preferably, metal containing layer 52 is substantially similar to metal containing layer 8 described above and may be of any of the same metals, alloys or compounds. If desired, a dielectric layer 51 can be formed on substrate 50 and beneath metal containing layer 52. Dielectric layer 51 is substantially similar to first dielectric layer 6 described above.

[0044] As illustrated in Figure 4, dielectric layer 54 is then deposited or otherwise formed on metal containing layer 52. Dielectric layer 54 may be any dielectric or insulating material used in IC device fabrication, such as those listed above for second dielectric layer 12. Preferably, dielectric layer 54 is silicon oxide or spin-on glass (SOG). Dielectric layer 54 may be formed by any IC device fabrication process giving the desired physical and chemical characteristics.

[0045] An aperture 56 such as a via or trench is then formed in dielectric layer 54 by removing a portion of dielectric layer 54 to expose underlying metal containing layer 52. Aperture 56 may be formed by any IC device manufacturing method, such as a photolithographic patterning and etching process.

[0046] As shown in Figure 5, metal containing collar 60 is formed on the sidewalls of aperture 56, using a spacer etch as known in the art. It will be understood that the term "collar" encompasses a co-parallel spacer structure 60 if aperture 56 is a trench extending over substrate 50. Similar to second metal containing layer 14, collar 60 may contain one or more metal containing layers with a single metal containing layer preferably used. Also in similar fashion to second metal containing layer 14, collar 60 may include not only metals, but their alloys and compounds. Like second metal containing layer 14, any metal can be employed in collar 60, provided it exhibits the desired characteristics, either alone or when combined with other metal containing layers, and the metals applicable to metal containing layer 14 are equally applicable to collar 60. Preferably, collar 60 comprises the same metal as metal containing layer 52. More preferably, when metal containing layer 52 comprises Al, collar 60 comprises Ti.

[0047] Collar 60 is formed by an IC device fabrication process which does not degrade metal containing layer 52, yet forms a collar or spacer-like structures 60 on the sidewall or sidewalls of aperture 56. For example, layer 61 (shown in Figure 4) of a material from which collar 60 is formed can be conformally deposited on dielectric layer 54 and the walls of aperture 56. Conformal coverage yields a substantially vertical sidewall in the dielectric aperture. While not preferred, a partially conformal layer of the material can be deposited instead. A highly conformal process is preferably employed to form layer 61. Portions of layer 61 on the bottom of aperture 56 and top of dielectric layer 54 are then removed, preferably by using an appropriate directional etch, such as reactive ion etching (RIE).

[0048] Conducting layer 62 is next deposited or otherwise formed to fill aperture 56 and extend over dielectric layer 54, as shown in broken lines in Figure 5. Conducting layer 62 may be deposited by any IC device fabrication method yielding the desired characteristics. For example, conducting layer 62 may be deposited by a conformal or non-conformal deposition process. An abrasive planarization process, such as chemical-mechanical planarization (CMP), is then used to remove portions above the horizontal plane of the upper surface of dielectric layer 54 and leave conductive plug (in a via 56) or line (in a trench 56) 64 as illustrated in Figure 6.

[0049] Similar to conducting layer 10, conducting layer 62 comprises any conducting material used in IC devices. Preferably, conducting layer 62 comprises aluminum, optionally containing other metals such as Si, W, Ti, and/or Cu. More preferably, conducting layer 62 is an aluminum-copper alloy. Conducting layer 62 may also comprise copper metal.

[0050] Dielectric layer 54 can then be optionally removed, thus forming the interconnect structure represented in Figure 7a. Dielectric layer 54 can be removed by any process which does not degrade any of metal containing layer 52, conducting layer 62, or collar 60. For example, when dielectric layer 54 is silicon oxide, it may be removed by an HF wet etch solution or an oxide dry etch process. If desired, portions of metal containing layer 52 can then be removed, preferably by a directional etching process, to obtain the interconnect structure shown in Figure 7b.

[0051] In an alternative method, upper metal containing layer 66 can be formed over conductive plug or line 64 as depicted in Figure 8. Like metal containing layer 52, upper metal containing layer 66 may contain one or more individual metal containing layers. Preferably, a single metal containing layer is used as upper metal containing layer 66. Similar to metal containing layer 52, upper metal containing layer 66 may contain not only metals but their alloys and compounds. Preferably, upper metal containing layer 66 comprises the same material as collar 60. More preferably, when conductive plug 64 comprises Al, upper metal containing layer 66 comprises Ti.

[0052] Upper metal containing layer 66 can be formed over conductive plug 64 in the following manner. Conducting layer 62 is deposited in aperture 56 and over dielectric layer 54 as described above with respect to Figure 5. Prior to completely filling aperture 56, however, the deposition of conducting layer 62 is halted as shown at 62a in Figure 5, leaving an upper portion of aperture 56 empty (i.e., a recess is left at the top of aperture 56). Upper metal containing layer 66 is then deposited over conducting layer 62, including the still-empty upper portion of aperture 56. Portions of conducting layer 62 and upper metal containing layer 66 above the horizontal plane of dielectric layer 54 are then removed by a planarization process, such as CMP, to form a completely enveloped, or clad, interconnect structure. If desired, portions of dielectric

layer 54 and metal containing layer 52 flanking the interconnect structure can be removed as described above to form the structure of Figure 9.

[0053] In another process variant, after forming metal containing layer 52 on substrate 50 and forming dielectric layer 54 with aperture 56 therethrough, but prior to forming collar 60, conductive plug or line 64 could be formed in aperture 56 as described above. Upper metal containing layer 66 could then be deposited, as described above, over conductive plug or line 64 and dielectric layer 54 to obtain the structure illustrated in Figure 10. Portions of upper metal containing layer 66 not overlying conductive plug or line 64 could then be removed by a photolithographic pattern and etch process, followed by removing dielectric layer 54 by the method described above, to obtain the structure illustrated in Figure 11. As explained above, the structure of Figure 11 could then have a conformed metal containing layer deposited and etched (similar to the deposition and etch of second metal containing layer 14 above) to form a structure similar to that depicted in Figure 3a.

[0054] While the preferred embodiments of the present invention have been described above, the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

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att. to sub spec

APPENDIX B

(VERSION OF SUBSTITUTE SPECIFICATION EXCLUDING CLAIMS
WITH MARKINGS TO SHOW CHANGES MADE)

(Serial No. 09/829,161)

PATENT
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APPLICATION FOR LETTERS PATENT

for

**METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE
INTERCONNECTS, METHODS FOR MAKING SAME, AND
SEMICONDUCTOR DEVICES INCLUDING SAME**

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TITLE OF THE INVENTION

METALLIZATION STRUCTURES FOR SEMICONDUCTOR DEVICE INTERCONNECTS,
METHODS FOR MAKING SAME, AND
SEMICONDUCTOR DEVICES INCLUDING SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of application Serial No. 09/388,031, filed September 1, 1999, pending.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: This invention relates generally to the field of semiconductor device design and fabrication. Specifically, the invention relates to methods for manufacturing metallization structures in integrated circuit devices and the resulting structures.

[0003] State of the Art: Integrated circuits (ICs) contain numerous individual devices, such as transistors and capacitors, that are interconnected by an intricate network of horizontal and vertical conductive lines commonly termed "interconnects." Exemplary interconnect structures are disclosed in U.S. Patent Nos. 5,545,590, 5,529,954, 5,300,813, 4,988,423, and 5,356,659, each of which patents is hereby incorporated herein by reference.

[0004] Aluminum interconnect structures are decreasing in size and pitch (spacing), as the industry trend continues toward, and includes, submicron features and pitches. The resultant reduction in structure sizes leads to numerous reliability concerns, including electromigration and stress voiding of the interconnect structures.

[0005] Stress notches (also known as stress voids) on the surface of conductive interconnect structures are of concern because the voids or notches degrade reliability and device performance. Stress notches, when formed in a conductive line, may render the line substantially discontinuous and unable to effectively transmit a signal. Stress notches at a grain boundary are extremely detrimental, as they may propagate along the boundary and sever the conductive line completely.

[0006] Stress notches are also undesirable because they can alter the resistivity of a conductive line and change the speed at which signals are transmitted. Resistivity changes from stress notching are especially important as line dimensions shrink, because notching in a submicron conductive line alters resistivity more than notching in a larger line with its consequently greater cross-sectional area. Thus, the ever more stringent pitch sizing and higher aspect ratios (height to width of the structure or feature) sought by practitioners in the art have imitated considerable stress voiding concerns.

[0007] It is believed that stress notching results from both structural and thermal stresses between conductive lines and adjacent insulating and passivation layers. Kordic et al., *Size and Volume Distributions of Thermally Induced Stress Voids in AlCu Metallization*, Appl. Phys. Lett., Vol. 68, No. 8, 19 February 1996, pp. 1060-1062, incorporated herein by reference, describes how stress voids begin at the edge of a conductive line where the density of the grain boundaries is largest. As illustrated in Figure 12 herein, stress notches form at the exterior surfaces and surface intersections of the conductive lines in order to relieve areas of high stress concentration. The notches may then propagate into, and across, the interior of the conductive line until the line becomes disrupted, cracked, and/or discontinuous.

[0008] Aluminum (Al) and Al alloy (such as Al/Cu) lines are especially susceptible to stress notching because of both the thermal expansion mismatch between Al and adjacent layers and the relatively low melting point of Al. As the temperature changes, stresses are induced in Al or Al alloy lines because aluminum's coefficient of thermal expansion (CTE) differs from the CTE of the materials comprising the adjacent layers. To relieve these stresses, Al atoms migrate and form stress notches. Further, because Al has a low melting point, Al atoms migrate easily at low temperatures and aggravate a tendency toward stress notch formation.

[0009] Several methods have been proposed to reduce stress notching. One proposed method uses a material less susceptible to stress notching, such as copper (Cu) or tungsten (W), in the conductive line. Using Cu in conductive lines, however, has in the past resulted in several problems. First, copper is difficult to etch. Second, adhesion between copper and adjacent insulating layers is poor and thus poses reliability concerns. Third, adding Cu to Al lines may reduce stress notching, but beyond a certain Cu concentration, device performance may begin to

degrade. Fourth, as conductive line geometries shrink, adding Cu to Al lines seems less effective in reducing stress notching. Finally, even using Cu interconnects in the manner employed in the prior art can still lead to notching effects, especially at $0.1 \mu\text{m}$ geometries and below since, at such dimensions, line widths have become so small that any imperfection can cause opens. Using W in Al conducting lines is also undesirable – W has a high resistivity and, therefore, reduces signal speed.

[0010] Another proposed method to reduce stress notching modifies how the layers adjacent conductive lines (e.g., insulating and passivation layers) are formed. This method has focused, without notable success, on the rate, temperature, and/or pressure at which the adjacent layers are deposited, as well as the chemical composition of such layers.

[0011] Yet another proposed method to reduce stress notching comprises forming a cap on the conductive lines. Such caps can be formed from TiN, W, or Ti-W compounds. These materials have higher melting points than Al and, therefore, have a higher resistance to stress notching. A disadvantage in using such caps, however, is that additional process steps, such as masking steps, are required.

[0012] U.S. Patent No. 5,317,185, incorporated herein by reference, describes still another proposed method for reducing stress notching. This patent discloses an IC device having a plurality of conductive lines where the outermost conductive line is a stress-reducing line. This stress-reducing line is a nonactive structure which reduces stress concentrations in the inner conductive lines.

BRIEF SUMMARY OF THE INVENTION

[0013] The present invention relates to a metallization structure for semiconductor device interconnects comprising a substrate having a substantially planar upper surface, a metal containing layer disposed on a portion of the substrate upper surface, a conducting layer overlying the metal containing layer, and metal containing spacers flanking the sidewalls of the conducting layer and the underlying metal containing layer. The metal containing layer and metal containing spacers do not encapsulate the conducting layer. The substrate upper surface is preferably a dielectric layer. The conducting layer preferably comprises aluminum or an

aluminum-copper alloy, but may also comprise copper. When the conducting layer comprises Al, the metal containing layer and metal containing spacer preferably comprise titanium, such as Ti or TiN. An optional dielectric layer, preferably silicon oxide, may be disposed on the conducting layer. When the optional dielectric layer is present, the metal containing spacer extends along the sidewall of the dielectric layer.

[0014] The present invention also relates to a metallization structure comprising a substrate having a metal containing layer disposed thereon, a dielectric layer having an aperture therethrough disposed on the substrate so the bottom of the aperture exposes the upper surface of the metal containing layer, at least one metal containing spacer on the sidewall of the aperture, and a conducting layer filling the remaining portion of the aperture. The metal containing layer and metal containing spacer preferably comprise titanium, such as Ti or TiN. At least one upper metal containing layer may be disposed on the conducting layer.

[0015] The present invention further relates to a method for making a metallization structure by forming a substantially planar first dielectric layer on a substrate, forming a metal containing layer over the first dielectric layer, forming a conducting layer over the metal containing layer, forming a second dielectric layer over the conducting layer, removing a portion of the second dielectric layer, conducting layer, and metal containing layer to form a multi-layer structure, and forming metal containing spacers on the sidewalls of the multi-layer structure. The process optionally removes both the second dielectric layer portion of the multi-layer structure and the laterally adjacent portions of the metal containing spacers.

[0016] The present invention additionally relates to a method for making a metallization structure by forming a substrate comprising a metal containing layer disposed thereon, forming a dielectric layer comprising an aperture on the substrate so the bottom of the aperture exposes the upper surface of the metal containing layer, forming a metal containing spacer on the sidewall (in the case of a via) or sidewalls (in the case of a trench) of the aperture, and forming a conducting layer in the remaining portion of the aperture. At least one upper metal containing layer may optionally be formed on the conducting layer.

[0017] The present invention also relates to a method for making a metallization structure by forming a substrate comprising a metal containing layer on the surface thereof,

forming on the substrate a dielectric layer comprising an aperture so the bottom of the aperture exposes the surface of the metal containing layer, forming a conducting layer in the aperture, forming an upper metal containing layer overlying the dielectric layer and the aperture, removing the portions of the upper metal containing layer overlying the dielectric layer, removing the dielectric layer, removing the portions of the metal containing layer not underlying the aperture to form a multi-layer metal containing structure, and forming a metal spacer on the sidewall or sidewalls of the multi-layer metal containing structure.

[0018] The present invention provides several advantages when compared to the prior art. One advantage is that thermally-induced stress voids are reduced because the metal containing layer and metal containing spacer comprise materials exhibiting good thermal-voiding avoidance characteristics. Another advantage is that the size of conductive lines can be shrunk further in comparison to dimensions achievable by conventional processes, since only one additional deposition and etch step, without an additional masking step, is needed to form the metallization structure. Shrinking of conductive lines is necessary as device geometries decrease to less than $0.1 \mu\text{m}$. At these small geometries, even small notches can significantly decrease conductivity.

[0019] The invention also specifically includes semiconductor devices including the inventive metallization structures.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0020] The present invention, in part, is illustrated by the accompanying drawings in which:

[0021] Figures 1, 2, 3a, and 3b illustrate cross-sectional views of one process of forming a metallization structure, and the structure formed thereby, according to the invention;

[0022] Figures 4, 5, 6, 7a, and 7b illustrate cross-sectional views of another process of forming a metallization structure, and the structure formed thereby, according to the invention;

[0023] Figures 8 and 9 illustrate cross-sectional views of yet another process of forming a metallization structure, and the structure formed thereby, according to the invention;

[0024] Figures 10 and 11 illustrate cross-sectional views of still another process of forming a metallization structure, and the structure formed thereby, according to the invention; and

[0025] Figure 12 illustrates a partial cross-sectional, perspective view of a conventional, prior art metallization structure exhibiting stress voids or notches.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Generally, the present invention relates to a metallization structure for interconnects and semiconductor devices including same. Specifically, the present invention reduces stress voiding, especially thermally induced stress voiding, in conducting lines. The metallization structures described below exemplify the present invention without reference to a specific device because the inventive process and structure can be modified by one of ordinary skill in the art for any desired device.

[0027] The following description provides specific details, such as material thicknesses and types, in order to provide a thorough description of the present invention. The skilled artisan, however, would understand that the present invention may be practiced without employing these specific details. Indeed, the present invention can be practiced in conjunction with conventional fabrication techniques employed in the industry.

[0028] The process steps described below do not form a complete process flow for manufacturing IC devices. Further, the metallization structures described below do not form a complete IC device. Only the process steps and structures necessary to understand the present invention are described below.

[0029] One embodiment of a process and resulting metallization structure of the present invention is illustrated in Figures 1, 2, 3a, and 3b. This embodiment may be characterized as a predominantly "subtractive" process, in comparison to the second embodiment discussed hereinafter, in that portions of superimposed material layers are removed to define the interconnect structure features, such as lines. As shown in Figure 1, a portion of semiconductor device 2 includes substrate 4 with overlying first dielectric layer 6. Substrate 4 may be any surface suitable for integrated circuit device formation, such as a silicon or other semiconductor

wafer or other substrate, and may be doped and/or include an epitaxial layer. Substrate 4 may also be an intermediate layer in a semiconductor device, such as a metal containing contact layer or an interlevel dielectric layer. Preferably, substrate 4 is a silicon wafer or bulk silicon region, such as a silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) structure.

[0030] First dielectric layer 6 may comprise any dielectric material used in IC device fabrication. Examples of such dielectric materials include silicon oxide, silicon nitride, silicon oxynitride, silicon oxide containing dopants such as boron (B) or phosphorus (P), organic dielectrics, or a layered dielectric film of these materials. Preferably, first dielectric layer 6 is silicon oxide or borophosphosilicate glass (BPSG). First dielectric layer 6 may be formed by any process yielding the desired physical and chemical characteristics, such as thermal oxidation, thermal nitridation, or vapor deposition.

[0031] Overlying first dielectric layer 6 is metal containing layer 8. One or more individual metal containing layers may be used as metal containing layer 8. For example, if two superimposed metal containing layers are employed (represented by the dashed line in metal containing layer 8), an adhesion-promoting metal containing layer can be a first, lower portion of metal containing layer 8 on first dielectric layer 6 and a stress-reducing layer can be a second, upper portion of metal containing layer 8. Other metal containing layers might be included for other functions, such as a layer for reducing electromigration. Preferably, a single metal containing layer is used as metal containing layer 8, especially when the single layer can reduce electromigration, function as an adhesion-promoting layer, and function as a stress-reducing layer. If two metal containing layers are employed, the first, upper metal containing layer may, for example, comprise tantalum, titanium, tungsten, TaN, or TiN and the second, lower metal containing layer overlying first dielectric layer 6 may, for example, comprise TiN, TiW, WN, or TaN.

[0032] Metal containing layer 8 includes not only metals, but their alloys and compounds (e.g., nitrides and silicides). For example, a metal containing layer containing titanium might also contain nitrogen or silicon, such as titanium nitride or titanium silicide. Any metal, metal alloy, or metal compound can be employed in metal containing layer 8, provided it exhibits the characteristics described above, either alone or when combined with other metal

containing layers. Examples of metals that can be employed in metal containing layer 8 include cobalt (Co), Ti, W, Ta, molybdenum (Mo), and alloys and compounds thereof, such as TiW or TiN. Preferably, metal containing layer 8 comprises titanium. Titanium is a good adhesion layer and serves as a stress-reducing layer since Ti exhibits good thermal voiding resistance characteristics.

[0033] Metal containing layer 8 is deposited or otherwise formed by any process used in IC device fabrication. For example, metal containing layer 8 may be deposited by chemical vapor deposition (CVD) or physical vapor deposition (PVD) techniques, depending on the characteristics required of the layer. As used herein, the term "CVD techniques" encompasses, without limitation, plasma-enhanced CVD, or PECVD. Preferably, when metal containing layer 8 is Ti, this layer is formed by sputtering (a form of PVD) a film of Ti. If metal containing layer 8 is a metal nitride, it may be formed, for example, by depositing the metal in a nitrogen-containing atmosphere or by depositing the metal and annealing in a nitrogen-containing atmosphere. If metal containing layer 8 is a metal silicide, it may be formed, for example, by first depositing either the metal containing layer or a silicon layer, then depositing the other, and heating to react the two layers and form the silicide. If metal containing layer 8 is a metal alloy, it may be formed by any process suitable for depositing the metal alloy. For example, either sputtering or CVD techniques can be employed.

[0034] Conducting layer 10 is then formed over metal containing layer 8. Conducting layer 10 may comprise any conducting material used in IC device fabrication. Preferably, conducting layer 10 comprises a conducting metal, such as Al, optionally containing other elements such as Si, W, Ti, and/or Cu. More preferably, conducting layer 10 is an aluminum-copper alloy. Conducting layer 10 may also be formed of Cu. Conducting layer 10 may be formed by any method used in IC device fabrication such as CVD or PVD techniques. Preferably, conducting layer 10 is deposited by a PVD method such as sputtering, as known in the art. Second dielectric layer 12 is next deposited or otherwise formed on top of conducting layer 10. Second dielectric layer 12 comprises any dielectric material used in IC device fabrication, including those listed above. Preferably, second dielectric layer 12 comprises a material that serves as an etch stop, as explained below. More preferably, second dielectric layer

12 comprises fluorine-doped silicon oxide or other low dielectric constant material. Second dielectric layer 12 may be formed by any suitable process giving the desired physical and chemical characteristics, such as CVD, PECVD (plasma enhanced chemical vapor deposition), spin-on methods, or otherwise, depending upon the dielectric material selected. For use of the preferred fluorine-doped silicon oxide, the preferred deposition method is PECVD.

[0035] As shown in Figure 2, portions of second dielectric layer 12, conducting layer 10, and metal containing layer 8 have been removed, forming multi-layer structure 13. The portions of layers 8, 10 and 12 are removed by any IC device fabrication process, such as a photolithographic patterning and dry etching process. The resulting multi-layer structure forms the basis for an interconnect structure according to the present invention. Of course, the patterning and etch process would normally be performed to define a large number of interconnect structures, such as conductive lines 100 (see Figures 3a and 3b) extending across substrate 4.

[0036] As also shown in Figure 2, second metal containing layer 14 (also termed a metal containing spacer layer) is then deposited on first dielectric layer 6 and over multi-layer structure 13. In similar fashion to the structure of metal containing layer 8, one or more individual metal containing layers, illustrated by the dashed line within second metal containing layer 14, may be used as second metal containing layer 14. Preferably, a single metal containing layer is used as second metal containing layer 14 for the same reasons as those set forth for metal containing layer 8.

[0037] Like metal containing layer 8, second metal containing layer 14 includes not only metals but their alloys and compounds (e.g., nitrides and silicides). Preferably, when conducting layer 10 comprises aluminum, second metal containing layer 14 comprises Ti. If conducting layer 10 comprises Cu, second metal containing layer 14 preferably comprises TiW. More preferably, second metal containing layer 14 comprises the same metal as metal containing layer 8. Second metal containing layer 14 may be deposited or otherwise formed by a process similar to the process used to form metal containing layer 8. Preferably, second metal containing layer 14 is formed by a conformal deposition process, such as CVD.

[0038] Next, as illustrated in Figure 3a, second metal containing layer 14 is spacer etched to remove portions of the second metal containing layer 14 on first dielectric layer 6 and on second dielectric layer 12, thereby leaving metal containing spacers 16 on the multi-layer structure 13. A spacer etch is a directional sputtering etch which removes second metal containing layer 14 so that metal containing spacers 16 remain on the sidewalls of multi-layer structure 13. The spacer etch uses the first and second dielectric layers as an etch stop.

[0039] If desired, second dielectric layer 12 can then be removed. Second dielectric layer 12 can be removed by any process which removes the second dielectric layer without removing first dielectric layer 6. If the first and second dielectric layers comprise different materials (e.g., when second dielectric layer 12 is silicon oxide and the first dielectric layer 6 is BPSG), any process which selectively etches the second dielectric layer 12 can be employed. The etch process would also remove the portions of metal containing spacers 16 laterally adjacent dielectric layer 12, thus resulting in the metallization structure illustrated in Figure 3b. When the first and second dielectric layers 6, 12 are similar or have similar etch rates (e.g., when both are silicon oxide or fluorine-doped), a facet etch process can be used. As shown in broken lines in Figure 3b, when the first and second dielectric layers 6 and 12 exhibit similar etch rates, the thickness of layer 6 will be reduced by substantially the thickness of removed layer 12.

[0040] The metallization structures illustrated in Figures 3a and 3b reduce thermally-induced stress voids in conductive lines 100. Metal containing layer 8 and metal containing spacers 16 serve as a protective coating at the respective lower and lateral surfaces of conductive lines 100 and at intersections thereof, thereby reducing the incidence of stress voids by preventing them from starting at these surfaces and intersections thereof on conductive line 100. Metal containing layer 8 and metal containing spacers 16 also increase reliability of conductive line 100 without reducing its resistance.

[0041] The metallization structures of Figures 3a and 3b can then be processed as desired to complete the IC device. For example, an interlevel dielectric layer could be deposited thereover, contact or via holes could be cut in the interlevel dielectric, a patterned metal containing layer could be formed to achieve a desired electrical interconnection pattern, and a protective dielectric overcoat deposited and patterned to expose desired bond pads.

[0042] Another embodiment of a process and resulting metallization structures of the present invention is represented in Figures 4 through 11. This embodiment may be characterized as more of an "additive" method or process than that described with respect to Figures 1 through 3b, in that metallization structures for interconnects are formed by deposition in apertures, such as vias or trenches. As such, it should be noted that cusping of material deposited to line the sidewall or sidewalls of an aperture may be of concern if the method of deposition is not sufficiently anisotropic or, in some instances, the aperture exhibits a very high aspect ratio. In Figure 4, metal containing layer 52 has been deposited or otherwise formed over substrate 50. Any of the substrates employable as substrate 4 above can be used as substrate 50. Preferably, substrate 50 is a silicon wafer or bulk silicon region, such as an SOI or SOS structure. Such substrate 50 can have active and passive devices and other electrical circuitry fabricated on it, these circuit structures being interconnected by the metallization structures of the present invention. Therefore, a direct electrical path may exist between the devices and circuitry of the substrate 50 (or 4), the devices and circuitry being omitted herein for simplicity.

[0043] Metal containing layer 52 may comprise a discrete conductive member, such as a wire, a stud, or a contact. Preferably, metal containing layer 52 is substantially similar to metal containing layer 8 described above and may be of any of the same metals, alloys or compounds. If desired, a dielectric layer 51 can be formed on substrate 50 and beneath metal containing layer 52. Dielectric layer 51 is substantially similar to first dielectric layer 6 described above.

[0044] As illustrated in Figure 4, dielectric layer 54 is then deposited or otherwise formed on metal containing layer 52. Dielectric layer 54 may be any dielectric or insulating material used in IC device fabrication, such as those listed above for second dielectric layer 12. Preferably, dielectric layer 54 is silicon oxide or spin-on glass (SOG). Dielectric layer 54 may be formed by any IC device fabrication process giving the desired physical and chemical characteristics.

[0045] An aperture 56 such as a via or trench is then formed in dielectric layer 54 by removing a portion of dielectric layer 54 to expose underlying metal containing layer 52. Aperture 56 may be formed by any IC device manufacturing method, such as a photolithographic patterning and etching process.

[0046] As shown in Figure 5, metal containing collar 60 is formed on the sidewalls of aperture 56, using a spacer etch as known in the art. It will be understood that the term "collar" encompasses a co-parallel spacer structure 60 if aperture 56 is a trench extending over substrate 50. Similar to second metal containing layer 14, collar 60 may contain one or more metal containing layers with a single metal containing layer preferably used. Also in similar fashion to second metal containing layer 14, collar 60 may include not only metals, but their alloys and compounds. Like second metal containing layer 14, any metal can be employed in collar 60, provided it exhibits the desired characteristics, either alone or when combined with other metal containing layers, and the metals applicable to metal containing layer 14 are equally applicable to collar 60. Preferably, collar 60 comprises the same metal as metal containing layer 52. More preferably, when metal containing layer 52 comprises Al, collar 60 comprises Ti.

[0047] Collar 60 is formed by an IC device fabrication process which does not degrade metal containing layer 52, yet forms a collar or spacer-like structures 60 on the sidewall or sidewalls of aperture 56. For example, layer 61 (shown in Figure 4) of a material from which collar 60 is formed can be conformally deposited on dielectric layer 54 and the walls of aperture 56. Conformal coverage yields a substantially vertical sidewall in the dielectric aperture. While not preferred, a partially conformal layer of the material can be deposited instead. A highly conformal process is preferably employed to form layer 61. Portions of layer 61 on the bottom of aperture 56 and top of dielectric layer 54 are then removed, preferably by using an appropriate directional etch, such as reactive ion etching (RIE).

[0048] Conducting layer 62 is next deposited or otherwise formed to fill aperture 56 and extend over dielectric layer 54, as shown in broken lines in Figure 5. Conducting layer 62 may be deposited by any IC device fabrication method yielding the desired characteristics. For example, conducting layer 62 may be deposited by a conformal or non-conformal deposition process. An abrasive planarization process, such as chemical-mechanical planarization (CMP), is then used to remove portions above the horizontal plane of the upper surface of dielectric layer 54 and leave conductive plug (in a via 56) or line (in a trench 56) 64 as illustrated in Figure 6.

[0049] Similar to conducting layer 10, conducting layer 62 comprises any conducting material used in IC devices. Preferably, conducting layer 62 comprises aluminum, optionally containing other metals such as Si, W, Ti, and/or Cu. More preferably, conducting layer 62 is an aluminum-copper alloy. Conducting layer 62 may also comprise copper metal.

[0050] Dielectric layer 54 can then be optionally removed, thus forming the interconnect structure represented in Figure 7a. Dielectric layer 54 can be removed by any process which does not degrade any of metal containing layer 52, conducting layer 62, or collar 60. For example, when dielectric layer 54 is silicon oxide, it may be removed by an HF wet etch solution or an oxide dry etch process. If desired, portions of metal containing layer 52 can then be removed, preferably by a directional etching process, to obtain the interconnect structure shown in Figure 7b.

[0051] In an alternative method, upper metal containing layer 66 can be formed over conductive plug or line 64 as depicted in Figure 8. Like metal containing layer 52, upper metal containing layer 66 may contain one or more individual metal containing layers. Preferably, a single metal containing layer is used as upper metal containing layer 66. Similar to metal containing layer 52, upper metal containing layer 66 may contain not only metals but their alloys and compounds. Preferably, upper metal containing layer 66 comprises the same material as collar 60. More preferably, when conductive plug 64 comprises Al, upper metal containing layer 66 comprises Ti.

[0052] Upper metal containing layer 66 can be formed over conductive plug 64 in the following manner. Conducting layer 62 is deposited in aperture 56 and over dielectric layer 54 as described above with respect to Figure 5. Prior to completely filling aperture 56, however, the deposition of conducting layer 62 is halted as shown at 62a in Figure 5, leaving an upper portion of aperture 56 empty (i.e., a recess is left at the top of aperture 56). Upper metal containing layer 66 is then deposited over conducting layer 62, including the still-empty upper portion of aperture 56. Portions of conducting layer 62 and upper metal containing layer 66 above the horizontal plane of dielectric layer 54 are then removed by a planarization process, such as CMP, to form a completely enveloped, or clad, interconnect structure. If desired, portions of dielectric layer 54

and metal containing layer 52 flanking the interconnect structure can be removed as described above to form the structure of Figure 9.

[0053] In another process variant, after forming metal containing layer 52 on substrate 50 and forming dielectric layer 54 with aperture 56 therethrough, but prior to forming collar 60, conductive plug or line 64 could be formed in aperture 56 as described above. Upper metal containing layer 66 could then be deposited, as described above, over conductive plug or line 64 and dielectric layer 54 to obtain the structure illustrated in Figure 10. Portions of upper metal containing layer 66 not overlying conductive plug or line 64 could then be removed by a photolithographic pattern and etch process, followed by removing dielectric layer 54 by the method described above, to obtain the structure illustrated in Figure 11. As explained above, the structure of Figure 11 could then have a conformed metal containing layer deposited and etched (similar to the deposition and etch of second metal containing layer 14 above) to form a structure similar to that depicted in Figure 3a.

[0054] While the preferred embodiments of the present invention have been described above, the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

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ABSTRACT OF THE DISCLOSURE

The present invention provides a metallization structure for semiconductor device interconnects such as a conductive line, including a substrate with a substantially planar upper surface, foundation metal containing layer disposed on a portion of the substrate upper surface, primary conducting metal containing layer overlying the foundation metal containing layer, and metal containing spacer on the sidewalls of the primary conducting metal containing layer and the foundation metal containing layer. The present invention also provides a metallization structure including a substrate with a foundation metal containing layer disposed thereon, a dielectric layer with an aperture therethrough being disposed on the substrate, where the bottom of the aperture exposes the foundation metal containing layer of the substrate, and a metal containing spacer on the sidewall of the aperture and a line or plug of a primary conducting metal to fill the remaining portion of the aperture. The present invention also includes methods for making the metallization structures.

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